REMARKS

Applicants appreciate the Office Action of August 25, 2004. Applicants have faxed a copy of the Klaus *et al.* reference to the Examiner as requested by the Examiner and respectfully request consideration of this reference. Claim 5 has been amended to recite "the method" as suggested by the Examiner and, therefore, Applicants respectfully submit that the objections with respect to this claim have been obviated. Claims 3, 7 and 11 have been amended to recite "an etchant" to remedy the antecedent basis problem pointed out by the Examiner. Thus, Applicants submit that Amended Claims 3, 7 and 11 are in compliance with 35 U.S.C. § 112. Applicants have amended Independent Claims 1, 5 and 9 as set out above and submit that the amended independent claims are patentable over the cited references for at least reasons discussed herein. Applicants have also amended Claims 2-4, 6-8 and 12 to correct typographical errors as well as bring these claims into conformity with the amendments to independent Claims 1, 5 and 9. Furthermore, Applicants have added new Claims 13-17 to the present application. Accordingly, Applicants respectfully submit that Claims 1-17 are in condition for allowance, which is respectfully requested in due course.

The Claim Objections Have Been Obviated

The Office Action objects to Claim 5 because the preamble of the Claim 5 recites "the structure" instead of "the method." *See* Office Action, page 3, paragraph 5. Applicants have amended Claim 5 to recite "the method" and, therefore, submit that the objection with respect to this claim has been obviated.

The Section 112 Rejections

Claims 3, 7 and 11 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. *See* Office Action, page 3, paragraph 6. Applicants have amended Claims 3, 7 and 11 to recite "an etchant" instead of "the etchant" and, therefore, submit that Claims 3, 7 and 11 are now in compliance with 35 U.S.C. § 112. Thus, Applicants respectfully request that the 112 rejections with respect to these claims be withdrawn.

The Section 102 Rejections

A. Amended Independent Claims 1 and 5 are Patentable

Claims 1-3 and 5-7 stand rejected under 35 U.S.C. § 102(b) as being anticipated by United States Patent No. 6,001,719 to Cho *et al.* (hereinafter "Cho"). Applicants respectfully submit that many of the recitations of the amended claims are neither disclosed nor suggested by Cho. For example, Amended Independent Claim 1, recites:

> A method of fabricating an integrated circuit device comprising:
> forming a conductive layer on a microelectronic substrate;
> **forming a first insulating layer** on the conductive layer, the first insulating layer including an overhanging portion that extends beyond the conductive layer;
> **forming a second insulating layer** on the microelectronic substrate to cover the first insulating layer; and
> **etching the second insulting layer to form a sidewall insulating region disposed laterally adjacent a sidewall of the conductive layer and extending between the overhanging portion of the first insulating layer and the microelectronic substrate**.

Amended Independent Claim 5 contains similar recitations to the highlighted recitations. Applicants respectfully submit that at least the highlighted portions of, for example, Amended Claim 1, are neither disclosed nor suggested by the cited reference for at least the reasons discussed below.

The Office Action points to Figures 2A through 2D of Cho as teaching all of the recitations of, for example, Claim 1. *See* Office Action, page 4, paragraph 7. In particular, the Office Action points to the shrinkage compensating oxide layer 135 as teaching the sidewall insulating region recited in the claims of the present invention. As recited in Cho:

> FIG. 2C is a sectional view showing the step of forming a shrinkage compensating oxide layer 135 (i.e., recessed spacer) and an interlayer insulating layer 140. In more detail, **the shrinkage compensating oxide layer 135 is formed on both side surfaces of the reduced silicide layer pattern 125a by thermally oxidizing the gate pattern after the cleaning process.** The thermal oxidation step is preferably carried out at a high-temperature, i.e., 800° C or more.

See Cho, column 3, lines 36-43 (emphasis added). Thus, the shrinkage compensating oxide layer 135 is formed by thermally oxidizing the gate pattern after the cleaning process. In contrast, Amended Claim 1 recites etching the second insulating layer to form the sidewall insulating region after the forming the second insulating layer. Nothing in Cho discloses or suggests at least the highlighted recitations of Amended Claim 1.

Accordingly, Independent Claims 1 and 5 are patentable over the cited reference for at least the reasons discussed above. Furthermore, the dependent claims are patentable over the cited reference at least per the patentability of the independent base claims from which they depend.

Many of the dependent claims are also separately patentable over Cho. For example, Claim 3 recites:

> The method according to Claim 1, wherein forming the conductive layer comprises forming the conductive layer **by adjusting an etchant so that the first insulating layer includes the overhanging portion that extends beyond the conductive layer.**

Claim 7 contains similar recitations. Nothing in Cho discloses or suggests the recitations of Claims 3 and 7. In particular, as discussed in Cho:

> As shown in FIG. 2B, the cleaning process is performed to remove polymer (not shown) generated on the face of the exposed semiconductor substrate and the surface of the gate pattern during the etching process for forming the gate pattern. **At this time, the silicide layer pattern 125 of FIG. 2A is partially removed through the cleaning process which results in a silicide layer pattern 125a whose left and right side surfaces are recessed.**

See Cho, column 3, lines 28-35 (emphasis added). Thus, Cho discusses recessing the left and right side surfaces of the silicide layer pattern 125a during the cleaning process to remove polymer generated on the face of the exposed semiconductor substrate and the surface of the gate pattern. In contrast, Claim 3 recites forming the conductive layer by adjusting an etchant such that the first insulating layer includes the overhanging portion that extends beyond the conductive layer. Accordingly, Claims 3 and 7 are separately patentable over the cited reference for at least these additional reasons.

B. Amended Independent Claims 1 and 5 are Patentable

Claims 1, 3-5, 7 and 8 stand rejected under 35 U.S.C. § 102(b) as being anticipated by United States Patent No. 5,262,352 to Woo *et al.* (hereinafter "Woo"). Applicants respectfully submit that many of the recitations of the amended claims are neither disclosed nor suggested by Woo. For example, Amended Independent Claim 1, recites:

> A method of fabricating an integrated circuit device comprising:
> forming a conductive layer on a microelectronic substrate;

> **forming a first insulating layer** on the conductive layer, the first insulating layer including an overhanging portion that extends beyond the conductive layer;
> **forming a second insulating layer** on the microelectronic substrate to cover the first insulating layer; and
> **etching the second insulting layer to form a sidewall insulating region disposed laterally adjacent a sidewall of the conductive layer and extending between the overhanging portion of the first insulating layer and the microelectronic substrate**.

Amended Independent Claim 5 contains similar recitations to the highlighted recitations of Amended Claim 1. Applicants respectfully submit that at least the highlighted portions of, for example, Amended Claim 1, are neither disclosed nor suggested by the cited reference for at least the reasons discussed below.

The Office Action points to Figures 1, 2, 15 and 16 of Woo as teaching all of the recitations of, for example, Claim 1. *See* Office Action, page 5, paragraph 8. As discussed in Woo:

> **To form the recessed sidewall portion 19a, the silicided layer 17 is etched in a first chemistry and the conductive layer 18 is etched in a second chemistry in a preferred form**. Dielectric layer 16 is RIE etched wherein the dielectric layer 20 and the overlying masking layer (not illustrated) are used to ensure that the etching of dielectric layer 16 does not form a recessed sidewall as illustrated. The opening 19 is etched in a selective manner so that the opening 19 exposes but does not completely remove silicided layer 15 and conductive layer 14.

See Woo, column 4, lines 42-45 (emphasis added). As further discussed in Woo:

> **In FIG. 3, a sidewall dielectric, referred to as sidewall spacer 22, is formed adjacent the recessed sidewall portion 19a.** Sidewall spacer 22 is formed as an oxide material, a nitride material, or a like insulator. Preferably, sidewall spacer 22 is a furnace TEOS or a low pressure chemical vapor deposition (LPCVD) silicon nitride layer.

See Woo, column 4, lines 66-68 (emphasis added). Thus, as discussed in Woo, the recessed sidewall portion 19a is formed by etching the silicide layer 17 in a first chemistry and by etching the conductive layer 18 in a second chemistry and a spacer 22 is provided on the recessed sidewall portion 19a of Woo. In contrast, the claims of the present invention recite forming a first insulating layer on the conductive layer having an overhanging portion that extends beyond the conductive layer and etching the second insulting layer to form **a sidewall insulating region** disposed laterally adjacent a sidewall of the conductive layer and

extending between the overhanging portion of the first insulating layer and the microelectronic substrate. Nothing in the Woo discloses or suggests the recitations of the claims of the present invention.

Accordingly, Independent Claims 1 and 5 are patentable over the cited reference for at least the reasons discussed above. Furthermore, the dependent claims are patentable over the cited reference at least per the patentability of the independent base claims from which they depend.

Many of the dependent claims are also separately patentable over Cho. For example, Claim 2 recites:

> The method according to Claim 1, further comprising:
> forming an insulating region between the overhanging portion of the first insulating layer and the microelectronic substrate; and
> **forming a sidewall spacer conforming to a sidewall of the first insulating layer, the sidewall insulating region and an adjoining surface of the insulating region.**

Nothing in Woo discloses or suggests at least the highlighted recitations of Claim 2. In particular, the spacer 22 is provided on the recessed sidewall portion 19a. In contrast, as recited in Claim 2, the spacer according to some embodiments of the present invention is formed to be conformed to the sidewall of the first insulating layer, the sidewall insulating region and the adjoining surface of the insulating region after the overhanging portion of the first insulating layer is covered with the sidewall insulating region by forming and etching the second insulating layer.

Furthermore, Woo further discusses that the sidewall oxide region 22 is formed by over-etching the spacer 22 using the RIE process. *See* column 9, lines 31-34. However, as described above, after the sidewall insulating region according to some embodiments of the present invention is formed adjacent to the conductive layer, the spacer of the present invention is formed to be conformed to the sidewall of the first insulating layer, the sidewall insulating portion and the adjoining surface of the insulating region as recited, for example, in Claim 2. Accordingly, Claim 2 is separately patentable over the cited reference for at least these additional reasons.

Accordingly, the recessed sidewall portion of Woo, the spacer of Woo and/or the sidewall oxide region of Woo do not disclose or suggest many of the recitations of the claims

of the present invention. Accordingly, Applicants submit that the Independent Claims 1 and 5 are patentable over the cited reference for at least the reasons discussed above. Furthermore, the dependent claims are patentable over the cited reference at least per the patentability of the independent base claims from which they depend.

The 103 Rejections

A. The Dependent Claims are Patentable

Claims 2 and 6 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Woo. Applicants respectfully disagree. As discussed above, the dependent claims are patentable at least per the patentability of the independent base claims from which they depend. Furthermore, Claims 2 and 6 are separately patentable over the cited references for the reasons discussed above with respect to Claim 2. In particular, as discussed above, the insulating region of Woo is formed adjacent the recessed sidewall portion by over-etching the spacer after the spacer is previously formed adjacent the recessed sidewall portion. In contrast, according to some embodiments of the present invention, the sidewall insulating region is previously formed adjacent to the sidewall of the conductive layer by forming the second insulating layer and successively etching the second insulating layer, and then the spacer is formed to be conformed to the sidewall of the first insulating layer and the sidewall insulating region. Accordingly, Claims 2 and 6 are separately patentable over the cited references for at least these additional reasons.

B. Claim 9 is Patentable over the Cited References

Claims 9, 11 and 12 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Woo in view of United States Patent No. 6,214,715 to Huang *et al.* (hereinafter "Huang"). Applicants respectfully disagree. For example, Amended Claim 9 recites:

> A method of fabricating an integrated circuit memory device, comprising:
> forming a first bit line comprising:
> forming a first conductive layer on a microelectronic substrate; and
> forming a first insulating layer on the first conductive layer, the first insulating layer including a first overhanging portion that extends beyond the first conductive layer; and
> forming a second bit line comprising:
> forming a second conductive layer on the microelectronic substrate; and

forming a second insulating layer on the second conductive layer, the second insulating layer including a second overhanging portion that extends beyond the second conductive layer;

forming a third insulating layer on the microelectronic substrate to cover the first and second bit lines; and

etching the third insulating layer to simultaneously form a first sidewall insulating layer region disposed laterally adjacent to a first sidewall of the first conductive layer, and a second sidewall insulating region disposed laterally adjacent to a second sidewall of the second conductive layer, wherein the first sidewall insulating region extends between the first overhanging portion of the first insulating layer and the microelectronic substrate, and the second sidewall insulating region extends between the second overhanging portion of the second insulating layer and the microelectronic substrate.

Applicants respectfully submit that at least the highlighted recitations of Claim 9 are neither disclosed nor suggested by the cited references.

The Office Action admits that Woo does not teach that the first and second conductive structures are first and second bit lines. *See* Office Action, page 9. However, the Office Action states that Huang provides the missing teachings. As discussed above, Woo discusses a sidewall oxide region that is formed by over-etching a spacer after the spacer is formed by etching a dielectric layer formed on the structure. In other words, the recessed sidewall portion of the conductive layer and silicide layer is primarily covered with the spacer, and then the remaining portion of the spacer after over-etching thereof makes the sidewall oxide region. Furthermore, when the sidewall oxide region is formed adjacent the recessed sidewall portion, the spacer is not formed on the recessed sidewall portion because the spacer is over-etched to thereby form the sidewall oxide region. In contrast, as recited in Claim 9 of present invention, the first sidewall insulating region and the second sidewall insulating region are simultaneously formed adjacent to the first sidewall of the first conductive layer and the second sidewall of the second conductive layer by forming a third insulating layer on the microelectronic substrate to cover the first bit line and the second bit line and etching the third insulating layer. The first sidewall spacer and the second sidewall spacer are formed to cover the first sidewall insulating region and the second sidewall insulating region, respectively, after completing the first sidewall insulating region and the second sidewall insulating region. Nothing in Woo discloses or suggests these recitations of the claims of the present invention.

Furthermore, although Huang discusses first and second conductive structures separated from each other by a self-aligned contact, the Huang reference teaches away from Woo regarding at least the sidewall oxide region formed by over-etching the spacer. Accordingly, none of the cited references, either alone or in combination, disclose or suggest many of the recitations of these claims. Furthermore, there is no motivation or suggestion to combine the cited references as suggested in the Office Action. As affirmed by the Court of Appeals for the Federal Circuit in *In re Sang-su Lee*, a factual question of motivation is material to patentability, **and cannot be resolved on subjective belief and unknown authority**. *See In re Sang-su Lee*, 277 F.3d 1338 (Fed. Cir. 2002). It is improper, in determining whether a person of ordinary skill would have been led to this combination of references, simply to "[use] that which the inventor taught against its teacher." *W.L. Gore v. Garlock, Inc.*, 721 F.2d 1540, 1553, 220 U.S.P.Q. 303, 312-13 (Fed. Cir. 1983).

The Office Action states:

> Since Woo and Huang are in the same field of endeavor, the purpose for which Huang is relied upon would have being [sic] recognized in Woo by one or ordinary skill in the art at the time the invention was made.

See Office Action, page 10. This motivation is a motivation based on "subjective belief and unknown authority", the type of motivation that was rejected by the Federal Circuit in *In re Sang-su Lee*. In other words, the Office Action does not point to any specific portion of the cited references that would induce one of skill in the art to combine the cited references as set forth in the Office Action. If the motivation provided in the Office Action is adequate to sustain the Office's burden of motivation, then anything that is in "the same field of endeavor" would render a combination obvious. This cannot be the case. Accordingly, the statement in the Office Action with respect to motivation does not adequately address the issue of motivation to combine as discussed in *In re Sang-su Lee*. Thus, it appears that the Office Action gains its alleged impetus or suggestion to combine the cited references by hindsight reasoning informed by Applicants' disclosure, which, as noted above, is an inappropriate basis for combining references.

Furthermore, the teachings of Woo and Huang are in complete disagreement regarding at least the sidewall oxide region, to the extent that making the modification proposed by the Examiner would render the invention of Woo inoperable. Thus, Applicants

submit, for this additional reason, one of ordinary skill in the art would not be motivated to combine the cited references to achieve the teachings of the present invention.

Accordingly, for at least these reasons, Applicants respectfully submit that Claim 9 and the claims that depend therefrom are patentable over the cited references and combinations thereof.

CONCLUSION

Applicants respectfully submit that pending claims are in condition for allowance for at least the reasons discussed above. Thus, allowance of the pending claims is respectfully requested in due course. Favorable examination and allowance of the present application is respectfully requested.

Respectfully submitted,

Elizabeth A. Stanek
Registration No. 48,568

USPTO Customer No. 20792
Myers Bigel Sibley & Sajovec
Post Office Box 37428
Raleigh, North Carolina 27627
Telephone: 919/854-1400
Facsimile: 919/854-1401

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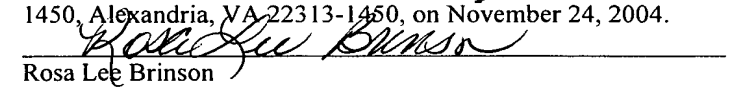

Rosa Lee Brinson